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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. ....09/820,468  
Filing Date ..... March 28, 2001  
Inventor .....Werner Juengling et al.  
Assignee ..... Micron Technology, Inc.  
Group Art Unit..... 2824  
Examiner .....Lebentritt, Michael  
Attorney's Docket No. ....MI22-1599  
Title: Methods of Forming Materials Between Conductive Electrical Components  
and Insulating Materials

**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**

To: Mail Stop RCE  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

From: Jennifer J. Taylor, Ph.D. (Tel. 509-624-4276; Fax 509-838-3424)  
Wells St. John P.S.  
601 W. First Avenue, Suite 1300  
Spokane, WA 99201-3828

Dear Sir:

The Examiner's attention is directed to the references which are listed on  
the attached Form PTO-1449 and copies of which are attached.

Citation of these references is respectfully requested.

Respectfully submitted,

Dated:

April 29, 2004

By:

Jennifer J. Taylor  
Jennifer J. Taylor, Ph.D.  
Reg. No. 48,711

**EL979979095**

0186  
PTO-140U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.  
MI22-1599SERIAL NO.  
09/820,468LIST OF ART CITED BY APPLICANT  
(Use several sheets if necessary)APPLICANT  
Werner Juengling et al.FILING DATE  
March 28, 2001GROUP  
2824

## U.S. PATENT DOCUMENTS

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	6,156,374	12-2000	Forbes et al.			
	AB	5,286,668	02-1994	Chou			
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						

## FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	AM							
	AN							
	AO							
	AP							
	AQ							

## OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

	AR		Stanley Wolf, "Silicon Processing for the VLSI Era", 1986, pp 1-8.
	AS		
	AT		
EXAMINER	DATE CONSIDERED		

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

EL465781655US



Inventor: Werner Juengling, et al.

Title: Methods of Forming Materials Between Conductive Electrical Components and Insulating Materials

Assignee: Micron Technology, Inc.

Priority Serial No. 09/115,339

Priority Filing Date: July 14, 1998

**INFORMATION DISCLOSURE STATEMENT**  
**PURSUANT TO 37 C.F.R. §§ 1.56, 1.97 AND 1.98**

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

The listed references were cited by, or submitted to, the Office in the parent, co-pending application of the above-identified application. The above-identified application is a divisional application of co-pending application Serial No. 09/115,339, filed July 14, 1998. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned. 37 C.F.R. § 1.98(d) and MPEP § 609(2).

Citation of these references is respectfully requested.

Respectfully submitted,

Dated: March 28, 2001

Attorney: Bernard Berman

Bernard Berman

Reg. No. 37,279

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**EL 979979095**

Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. M122-1599		PRIORITY SERIAL NO. 09/115,339	
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Werner Juengling et al.			
APR 29 2004 PATENT				PRIORITY FILING DATE July 14, 1998		PRIORITY GROUP 2813	
U.S. PATENT DOCUMENTS							
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
AA	3,919,060	11/11/75	Pogge et al.				
AB	3,979,230	9/7/76	Anthony et al.				
AC	3,998,662	12/21/76	Anthony et al.				
AD	4,063,901	12/20/77	Shiba				
AE	4,180,416	12/25/79	Brock				
AF	5,488,015	1/30/96H	evemann et al.				
AG	5,496,773	3/5/96	Rhodes et al.				
AH	5,525,857	6/11/96G	nade et al.				
AI	5,527,737	6/18/96J	eng				
AJ	5,583,078	12/10/96	Osenbach				
AK	5,599,745	2/4/97	Reinberg				
FOREIGN PATENT DOCUMENTS							
Document Number	Date	Country	Class	Subclass	Translation		
					Yes	No	
AL							
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AO							
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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
AR	HOMMA, TETSUYA. "Low Dielectric Constant Materials and Methods for Interlayer Dielectric Films in Ultralarge-Scale Integrated Circuit Multilevel Interconnections", <u>Materials Science &amp; Engineering</u> , R23, pp. 243-285 (1998)						
AS	ABSTRACT: Townsend, P.H., et al., "SiLK Polymer Coating With Low Dielectric Constant and High Thermal Stability for ULSI Interlayer Dielectric", <u>The Dow Chemical Company</u> , Midland, MI, 9 Pages, (Undated)						
AT	PRODUCT BROCHURE and MATERIAL SAFETY DATA SHEET, "Interlayer Dielectric", <u>JSR Microelectronics</u> , 12 Pages (1997)						
EXAMINER				DATE CONSIDERED			
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

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LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Werner Juengling et al.			
APR 29 2004 PATENT				PRIORITY FILING DATE July 14, 1998		PRIORITY GROUP 2813	
U.S. PATENT DOCUMENTS							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,629,238	5/13/97C	hoi et al.			
	AB	5,670,828	9/23/97C	beung et al.			
	AC	5,691,565	11/25/97	Manning			
	AD	5,691,573	11/25/97	Avanzino et al.			
	AE	5,773,363	6/30/98D	erderian et al.			
	AF	3,954,523	05/76	Magdo et al.	148	175	
	AG	5,023,200	06/91	Blewer et al.	437	187	
	AH	5,470,801	11/95	Kapoor et al.	437	238	
	AI	5,192,834	03/1993	Yamanishi et al.			
	AJ	5,461,003	10/1995	Havemann et al.			
	AK	5,744,399	04/1998	Rostoker et al.			
FOREIGN PATENT DOCUMENTS							
		Document Number	Date	Country	Class	Subclass	Translation
							Yes      No
	AL						
	AM						
	AN						
	AO						
	AP						
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
	AR		Togo, M., "A Gate-side Air-gap Structure (GAS) to Reduce the Parasitic Capacitance in MOSFETs", 1996 Sympos. on VLSI Technology Digest of Technical Papers, IEEE 1996, pp. 38-39.				
	AS		Anand, M.B., "NURA: A Feasible, Gas-Dielectric Interconnect Process", 1996 Sympos. on VLSI Technology Digest of Technical Papers, IEEE 1996, PP. 82-83.				
	AT		Watanabe, H., "A Novel Stacked Capacitor with Porous-Si Electrodes for High Density DRAMs", Microelectronics Research Laboratories, NEC Corp., date unknown, pp. 17-18.				
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

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Form PTO-1599		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. MI22-1599		PRIORITY SERIAL NO. 09/115.339	
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Werner Juengling et al.		PRIORITY FILING DATE July 14, 1998	
APR 29 2004 PATENT OFFICE				PRIORITY GROUP 2813			
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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,171,713	12/1992	Mathews			
	AB	4,561,173	12/1985	TeVelde			
	AC	5,141,896	08/1992	Katoh			
	AD	5,736,425	04/1998	Smith et al.			
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	AK	5,883,014	03/1999	Chen et al.			
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	AM	6,001,747	12/1999	Annapragada			
	AN	S/N 09/948,372		Leonard Forbes et al.			10/9/97
FOREIGN PATENT DOCUMENTS							
		Document Number	Date	Country	Class	Subclass	Translation
							Yes No
	AO						
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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
	AQ	Peter Singer (Editor-in-Chief); "The New Low-k Candidate: It's a Gas"; Technology News, March 1989, 1 page					
	AR	ABSTRACT: Anderson, R.C. et. al., "Porous Polycrystalline Silicon: A New Material For MEMS", Jnl. Of Microelectromechanical Systems (Mar. 1994), Vol. 3, No. 1, pp. 10-18					
	AS	Stanley Wolf, "Silicon Processing for the VLSI Era", Vol. 1, Sunset Beach, CA; Lattice Press, pp. 429-437.					
EXAMINER				DATE CONSIDERED			
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